DOCKET NO. P05411 **PATENT**
CLIENT NO. NATI15-05411
Customer No. 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Moshe Alon
Serial No.:	10/797,478
Filed:	March 10, 2004
For:	CLOCK FREQUENCY MONITOR
Group No.:	2816
Examiner:	An T. Luu

MAIL STOP APPEAL BRIEF-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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1. Appeal Brief;
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3. Petition for 2 Mo. Extension;
3. Check in the amount of $950.00 for the Appeal Brief filing fee ($500.00); and ($450.00) 2 mo. extension fee, and
4.. A postcard receipt;

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to MAIL STOP APPEAL BRIEF-Patents, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on November 6, 2006.

Date: 11/6/06 Nancy Hamberti
Mailer

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PTO/SB/17 (12-04)
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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 950.00

Complete if Known	
Application Number	10/797,478
Filing Date	March 10, 2004
First Named Inventor	Moshe Alon
Examiner Name	An T. Luu
Art Unit	2816
Attorney Docket No.	P05411

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0208 Deposit Account Name: Munck Butrus P.C.

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____ x	_____ =	_____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____ x	_____ =	_____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number) x	_____ =	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: Appeal Brief filing feee ($500.00) and Extension of Time Fee ($450.00)	$950.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 39,308	Telephone 972-628-3600
Name (Print/Type)	William A. Munck		Date Nov 6, 2006

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MAIL STOP APPEAL BRIEF - PATENTS
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APPEAL BRIEF

The Appellant has appealed to the Board of Patent Appeals and Interferences from the final rejection mailed December 30, 2005 and the Advisory Action mailed May 17, 2006, rejecting Claims 1-28. The Appellant filed a Notice of Appeal and a Pre-Appeal Brief request for review on May 24, 2006, and a Panel Decision was mailed August 4, 2006. The Appellant respectfully submits this brief on appeal with the appropriate statutory fee, along with the fee and a request for a two-month extension of time.

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Real Party in Interest

The real party in interest and assignee of this case is National Semiconductor Corporation.

Related Appeals or Interferences

To the best knowledge and belief of the undersigned attorney, there are none.

Status of Claims

Claims 1-28 have been finally rejected pursuant to the Office Action dated December 30, 2005 and Advisory Action dated May 17, 2006. Claims 1-28 are presented on appeal. A copy of all pending claims is provided in Appendix A.

Status of Amendments after Final

An AMENDMENT AND RESPONSE TO OFFICE ACTION was filed on May 24, 2006. According to the Advisory Action dated May 17, 2006, the Examiner did not enter amendments after final rejection. Applicant notes that no amendments were made after final rejection, although Claim 9 was erroneously listed as "currently amended," and the amendments to that claim shown were those made in a response filed November 9, 2005 and were entered.

The Claims Appendix (Appendix A) shows the current, correct state of the claims after the amendment filed and entered on November 9, 2005, prior to the final rejection mailed December 30, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

The following summary refers to disclosed embodiments and their advantages but does not delimit any of the claimed inventions.

In General

The present application includes a frequency monitor circuit (FMC) that is part of an integrated-circuit chip for monitoring the frequency of one or more clocks present on the chip. The FMC includes (i) a reference window generator operative to output a reference window signal of a given duration and (ii) a clock counter operative to count all pulses, in any one of the clocks, that occur within the duration of the reference window and to output a corresponding pulse count. The FMC further includes two or more comparators, each operative to compare the pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation. In one configuration in which the clock is generated on the chip by a frequency multiplier, the reference window generator and the clock counter are shared between the frequency monitor circuit and the frequency multiplier. *Abstract.*

Support for Independent Claims

Note that, per 37 CFR §41.37, only each of the independent claims is discussed in this section. In the arguments below, however, the dependent claims are also discussed and distinguished from the prior art. The discussion of the claims is for illustrative purposes, and is not intended to affect the scope of the claims.

Independent Claim 1 describes a frequency monitor circuit (FMC) 10 configured to receive at least one monitored clock whose frequency is to be monitored. The FMC includes a reference window generator (RWG) 12 operative to output a reference window signal defining a reference window, the reference window having a given duration. The FMC also includes a monitored clock counter (MCC) 14 operative to count all pulses in any one of the at least one monitored clock that occur within the duration of the reference window and to output a corresponding pulse count. The FMC also includes at least two comparators 16, each comparator operative to compare the pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation. *Page 3, lines 12-24; and Figures 1A and 1B. Figure 1A is reproduced next page.*

Independent Claim 15 describes an integrated circuit chip, on which there is provided at least one monitored clock whose frequency is to be monitored, including a frequency monitor circuit (FMC) 10. The FMC includes a reference window generator (RWG) 12 operative to output a reference window signal defining a reference window, the reference window having a given duration. The FMC also includes a monitored clock counter (MCC) 14 operative to count all pulses in any one of the at least one monitored clock that occur within the duration of the reference window and to output a corresponding pulse count. The FMC also includes at least two comparators 16, each comparator operative to compare the pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation. *Page 3 lines 12-24; and Figures 1A and 1B.*

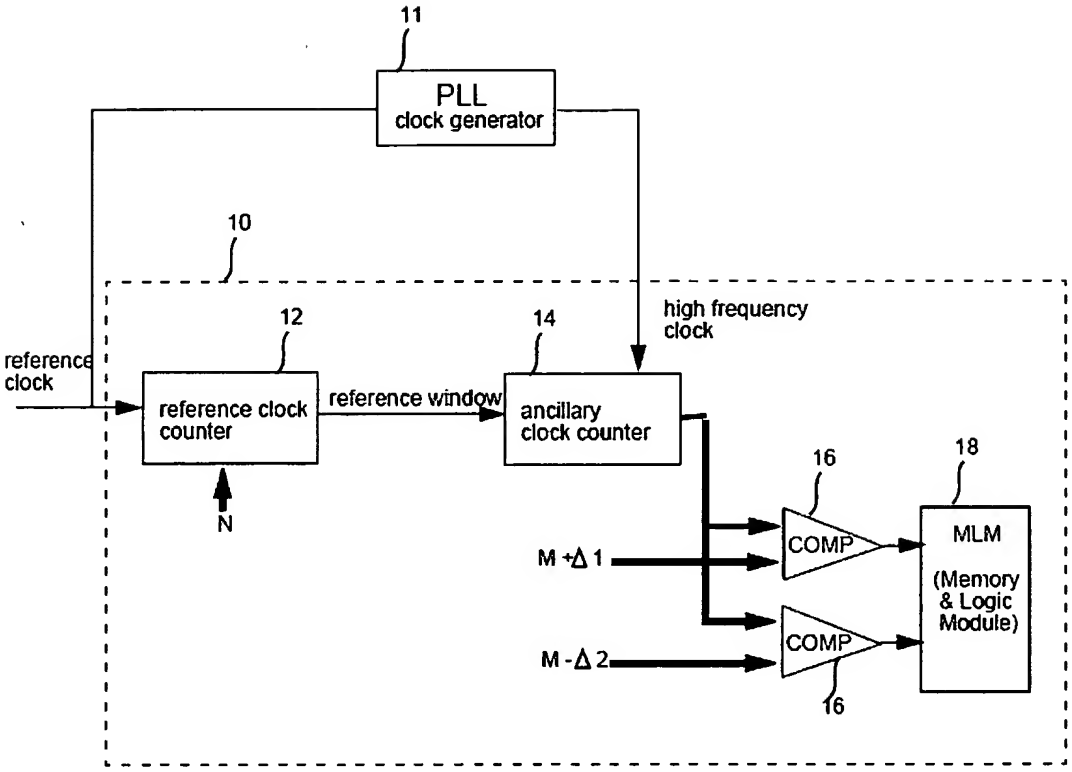
11
PLL
clock generator
10
12
14
high frequency
clock
reference
clock
reference clock
counter
reference window
ancillary
clock counter
16
18
COMP
MLM
(Memory
& Logic
Module)
N
M +Δ 1
M -Δ 2
COMP
16

FIG.1A

Grounds of Rejection to be Reviewed on Appeal

1. Are Claims 1-10, and 15-24 obvious over Applicant's Admitted Prior Art (APA) in view of U.S. Patent No. 6,289,055 to Knotz ("Knotz")?

2. Are Claims 11-14 and 25-28 obvious over Applicant's Admitted Prior Art (APA) in view of U.S. Patent No. 6,289,055 to Knotz ("Knotz") in further view of U.S. Patent No. 6,542,013 to Volk, *et al.* ("Volk")?

ARGUMENT

Stated Grounds of Rejection

The rejections outstanding against the Claims are as follows:

1. Claims 1-10 and 15-24 were rejected under 35 U.S.C. 103(a) as obvious over Applicant's Admitted Prior Art (APA) in view of U.S. Patent No. 6,289,055 to Knotz ("Knotz").

2. Claims 11-14 and 25-28 were rejected under 35 U.S.C. 103(a) as obvious over Applicant's Admitted Prior Art (APA) in view of U.S. Patent No. 6,289,055 to Knotz ("Knotz") in further view of U.S. Patent No. 6,542,013 to Volk, *et al.* ("Volk").

Legal Standards

The legal standards for an obviousness[1] rejection are referenced in the footnote below.

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[1]The Supreme Court has explained how to apply §103:

> Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or non-obviousness of the subject matter is determined.
>
> *Graham v. John Deere Co.*, 383 U.S. 1, 148 U.S.P.Q. 459, 467 (1966).

Obviousness cannot be inferred from a combination of references without a showing that one of ordinary skill would have been motivated to combine those references:

> When prior art references require selective combination ... to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention

(continued...)

Analysis of Examiner's Rejection

The cited references are each briefly discussed in relevant part, and then the rejection of each claim is addressed separately under each ground of rejection.

Applicant's Admitted Prior Art (APA) refers to prior art Figure 2 of the instant application; Examiner Luu also uses the generic "FIG. 2" to reference APA in the Office Action portions cited below. Figure 2 shows, in block diagram form, a typical frequency multiplier (Fmul) type of a clock generator known from the prior art. It is seen to comprise a high-frequency pulse train generator (HFPG) 21, frequency control logic 23, a reference clock counter (RCC) 22, a high-frequency clock counter (HFCC) 24 and a comparator 27, all interconnected as shown. RCC 22 receives a reference clock and a window count value N; comparator 26 receives, as a comparison value, a nominal high-frequency count value M. In operation, RCC 22 counts a number of successive reference clock pulses equal to the given window count N and outputs a reference window signal over the duration of this counting. The reference window signal is applied to HFCC 24, which counts successive pulses in the high-frequency clock, output by HFPG 21, over the duration of the reference window. The count from the HFCC is applied to comparator 27, which compares it with M. As a result, the

---

[1](...continued)

> itself.... Something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination.
>
> *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 5 U.S.P.Q.2d 1434, 1438 (Fed.Cir. 1988), *quoting Interconnect Planning Corp. v. Feil*, 227 U.S.P.Q. 543 (Fed.Cir. 1985), *and Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick*, 221 U.S.P.Q. 481 (Fed.Cir. 1984).

comparator outputs a signal indicating whether the count exceeds or falls below M. This signal is applied to frequency control logic 23, which accordingly corrects the frequency control value that it continuously sends to pulse train generator 21. This operational cycle is repeated indefinitely.

Knotz describes a method for transmitting signals but does not teach or suggest significant limitations of the claims, as will be discussed in detail below. For example, Knotz does not teach or suggest anything related to frequency deviation (and in fact does not mention frequency at all) as required by the claims.

Volk describes fractional divisors for multiple-phase PLL systems but does not teach or suggest significant limitations of the claims as will be discussed in detail below. For example, Volk does not teach or suggest anything related to frequency deviation as required by the claims.

Ground of Rejection 1: Claims 1-10 and 15-24 were rejected under 35 U.S.C. 103(a) as obvious over Applicant's Admitted Prior Art (APA) in view of U.S. Patent No. 6,289,055 to Knotz ("Knotz").

These claims are allowable over this combination of references as discussed below.

Claim 1

Independent Claim 1 recites, among other limitations, "at least two comparators, each comparator operative to compare said pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation". Applicant notes that this specific feature provides advantages over the prior art implementations. APA does not teach or suggest this particular limitation, as Examiner Luu acknowledges, nor does APA itself include any teaching or suggestion that such a dual-comparator solution would be useful or advantageous or any motivation to look to any other art for any purpose.

Examiner Luu looks to Knotz to satisfy this limitation, stating:

Knotz discloses in figure 2 an apparatus comprising a pulse signal circuit 1 to produce a pulse count and at least two comparators (31 and 32), responsive to said pulse count (i.e., signal on line 2), each comparator being operative to compare said pulse count with a respective given threshold value (i.e., voltage value V1 and V2 and to output a corresponding indication of frequency deviation (S31 and S32) as required by the claim.

Examiner Luu is incorrect. Knotz's Figure 2 is depicted below.

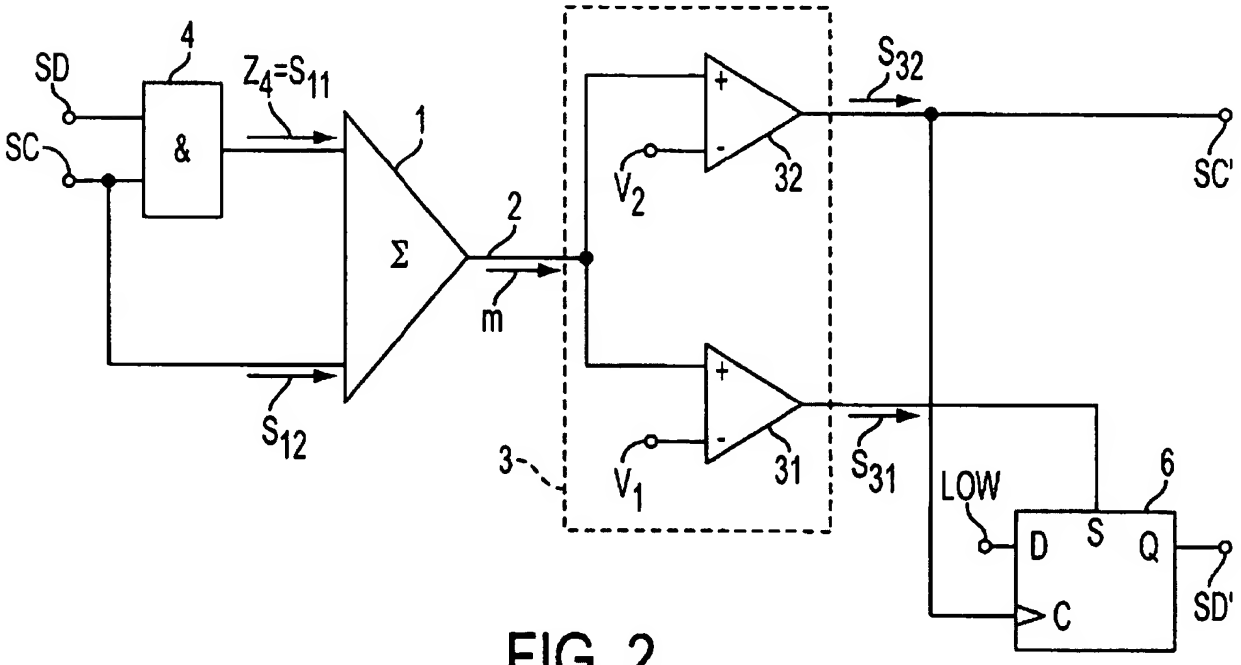

FIG. 2

Knotz teaches at col. 3, lines 52-65:

The multilevel signal m is transmitted through the signal lead 2 to the receiver unit 3 where It is compared in the first comparator 31 with the first signal threshold V_1 above the middle logical signal level H_1, and in the second comparator 32 With the second signal threshold V_2 below the middle logical signal level H_1. As the result of comparison, the first comparator 31 supplies the first digital received signal s_{31} corresponding to the first digital transmission signal s_{11} and the second comparator 32 supplies the regenerated clock signal SC', i.e.,

> the second digital received signal s_{32} corresponding to the second digital transmission signal s_{12} and equal to the clock signal SC.

Knotz also teaches at col. 3, lines 24-32 (emphasis added):

> For amplitude filtering in the receiver unit 3, one comparator 31, 32, ... 3n is provided for each of the digital transmission signals s_{11}, sS_{12} ... s_{1n} respectively to compare the multilevel signal m with in each case one signal threshold V_1, V_2, ... V_n respectively between two adjacent logical signal levels of the multilevel signal m, and to supply as comparison result the digital received signal s_{31}, s_{32}, ... s_{3n} corresponding to the respective digital transmission signal s_{11}, s_{12}, ... s_{1n}..

As can be clearly seen, each of the comparators 31-3n of Knotz simply generates an output by comparing a voltage of the multilevel signal m to a reference voltage. However, the outputs of the comparators 31-3n in no way represent an "indication of frequency deviation" as required by the claim. As clearly shown in Figure 3 of Knotz, the different reference voltages of Knotz simply represent possible voltage levels within the multilevel signal m. The different reference voltages of Knotz are not used in any way to indicate a "frequency deviation" of a signal. As a result, Knotz fails to disclose, teach, or suggest "at least two comparators," each of which is operative "to compare [a] pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation" as recited in Claim 1.

The comparators 31-3n of Knotz are used for a purpose completely unrelated to any function of APA. The comparators 31-3n of Knotz are specifically used to allow multiple digital signals to be summed and transmitted over a single lead. The comparators 31-3n of Knotz must be used in order for the multiple digital signals to be recovered from the multilevel signal m at the receiver 3. This functionality is not needed in APA in any way. The high frequency clock counter 24 of APA outputs a single value to the comparator 27. APA never teaches or suggests that the high frequency clock counter 24 needs to simultaneously output multiple values over a single lead. As a result, there is no need, teaching, or suggestion to incorporate the comparators 31-3n of Knotz into the system

of APA. Knotz's Figure 3 shows signal s31, the output of comparator 31, as compared to signal m, the input to comparator 31:

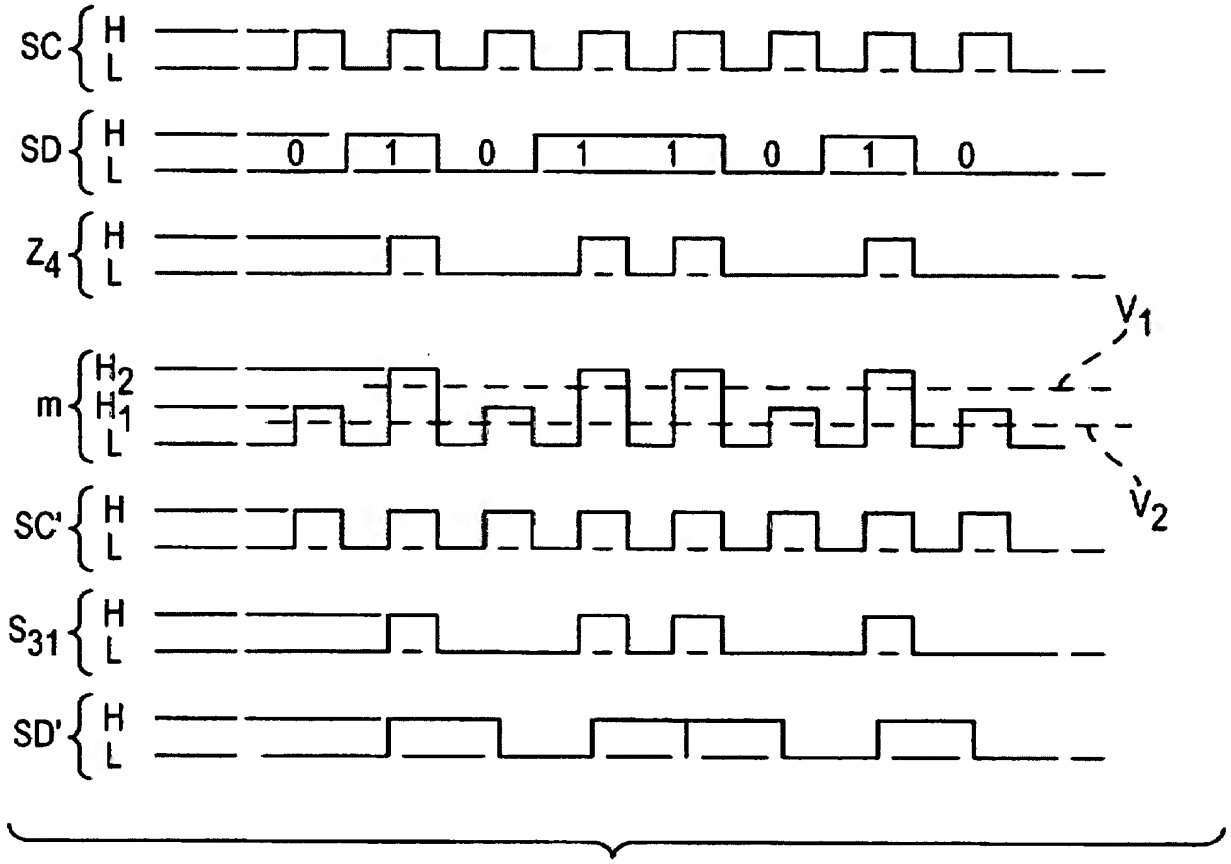

FIG. 3

Examiner Luu's response in the final Office Action indicates that the Examiner misunderstands the teachings of Knotz. Knotz clearly teaches in col. 3, lines 24-32 (reproduced above) that the comparators function to provide an amplitude filtering of the multilevel signal m. As can be seen, the signals s31, s32, . . . s3n are the result of an amplitude filtering - also illustrated clearly in Knotz's Figure 3 - and have nothing to do with an "indication of frequency deviation." Knotz does not teach or suggest anything related to frequency deviation, and in fact does not mention frequency at all.

Examiner Luu also states, incorrectly and without basis, that "figure 3 of Knotz clearly indicates a frequency that a reference signal (i.e., signal m) is above a first threshold V1 (i.e. signal S31) and a frequency that a reference signal is above a second threshold V2 (i.e. signal SC'). Therefore, the outputs of the comparators indicate changes of the frequency of the input signal with respect to predetermined values V1 and V2" (page 6, second paragraph of final Office Action). Signal m is amplitude filtered, and the voltage thresholds are not at all compared with the frequency of signal m. Examiner Luu evidently confuses amplitude and frequency in Knotz's teachings and has been unable or unwilling to clarify this reasoning.

Independent Claim 1 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 2

Claim 2 requires, among other limitations, "a storage and logic module (SLM), wherein said RWG, said MCC and said comparators are operative to function repeatedly and the SLM is operative to store one or more indications output by the comparators, the one or more stored indications being available for readout".

This limitation is not taught or suggested by any combination of APA and Knotz in combination with the limitations of the parent claim. As Claim 2 depends from Claim 1, the arguments above with regard to Claim 1 apply here as well and are incorporated herein by reference.

Claim 2 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 3

Claim 3 requires, among other limitations, that the "SLM is further operative to process the stored indications so as to obtain statistical information about the frequency of any of the at least one monitored clock".

This limitation is not taught or suggested by any combination of APA and Knotz, particularly in combination with the limitations of the parent claim. As Claim 3 depends from Claim 2, the arguments above with regard to Claims 1 and 2 apply here as well and are incorporated herein by reference.

In the rejection of Claim 2, Examiner Luu alleged that Knotz's element 6 functioned as the claimed storage and logic module (SLM). Examiner Luu then admits that the limitations of Claim 3 are not met:

> As to claims 3 and 4, element 6 of Knotz is a simple latch wherein information is process [*sic*] based on one parameter (i.e., Data input at node D). However, it is common nowadays to have a simple miniature processor to analyze data for statistically [*sic*] purposes. This it would have been obvious to one of skill in the art to replace a simple latch with an off-the-shelf processor to process information or data as required by the claim.

Examiner Luu's argument has numerous problems. First, nothing in any art of reference teaches or suggests the desirability of making a modification to replace Knotz's latch with a processor. The only motivation suggested by Examiner Luu is "to process information or data as required by the claim," a clear indication of improper hindsight reasoning. Finally, Examiner Luu only alleges that the use of such a processor is "common nowadays". This does not even meet the requirements for a *prima facie* obviousness rejection, which requires an examination of the knowledge of one of ordinary skill in the art at the time the invention was made, not "nowadays" as the claim is being examined.

Claim 3 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 4

Claim 4 requires, among other limitations, that the "statistical information includes indication of a trend in frequency deviation".

This limitation is not taught or suggested by any combination of APA and Knotz, particularly in combination with the limitations of the parent claim. As Claim 4 depends from Claim 3, the arguments above with regard to Claims 1, 2, and 3 apply here as well and are incorporated herein by reference.

Neither Knotz nor APA teaches or suggests anything related to frequency deviation, nor anything related to statistical information at all.

Claim 4 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 5

Claim 5 requires, among other limitations, "at least one clock generator, an output of any of said at least one clock generator being one of the at least one monitored clock".

This limitation is not taught or suggested by any combination of APA and Knotz in combination with the limitations of the parent claim. As Claim 5 depends from Claim 1, the arguments above with regard to Claim 1 apply here as well and are incorporated herein by reference.

Claim 5 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 6

Claim 6 requires, among other limitations, that the "at least one clock generator comprises a phased locked loop (PLL)".

This limitation is not taught or suggested by any combination of APA and Knotz, particularly in combination with the limitations of the parent claim. As Claim 6 depends from Claim 5, the arguments above with regard to Claims 1 and 5apply here as well and are incorporated herein by reference.

Claim 6 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 7

Claim 7 requires, among other limitations, that the "at least one clock generator is a frequency multiplier".

This limitation is not taught or suggested by any combination of APA and Knotz, particularly in combination with the limitations of the parent claim. As Claim 7 depends from Claim 5, the arguments above with regard to Claims 1 and 5 apply here as well and are incorporated herein by reference.

Claim 7 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 8

Claim 8 requires, among other limitations, "said RWG and said MCC form part of said frequency multiplier".

This limitation is not taught or suggested by any combination of APA and Knotz, particularly in combination with the limitations of the parent claim. As Claim 8 depends from Claim 7, the arguments above with regard to Claims 1, 5, and 7 apply here as well and are incorporated herein by reference.

Claim 8 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 9

Claim 9 requires, among other limitations, that "said RWG includes a reference clock counter (RCC) operative to count a given number of reference clock pulses in a reference clock, and wherein a beginning of said reference window coincides with a beginning of said counting and an end of said reference window coincides with an end of said counting".

This limitation is not taught or suggested by any combination of APA and Knotz in combination with the limitations of the parent claim. As Claim 9 depends from Claim 1, the arguments above with regard to Claim 1 apply here as well and are incorporated herein by reference.

Claim 9 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 15

Independent Claim 15 requires, among other limitations, "at least two comparators, each comparator operative to compare said pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation". Applicant notes that this specific feature provides advantages over the prior art implementations. APA does not teach or suggest this particular limitation, as Examiner Luu acknowledges, nor does APA itself include any teaching or suggestion that such a dual-comparator solution would be useful or advantageous, or any motivation to look to any other art for any purpose.

Examiner Luu looks to Knotz to satisfy this limitation, stating:

> Knotz discloses in figure 2 an apparatus comprising a pulse signal circuit 1 to produce a pulse count and at least two comparators (31 and 32), responsive to said pulse count (i.e., signal on line 2), each

> comparator being operative to compare said pulse count with a respective given threshold value (i.e., voltage value V1 and V2 and to output a corresponding indication of frequency deviation (S31 and S32) as required by the claim.

Examiner Luu is incorrect, as illustrated by Knotz's Figure 2, reproduced above with relation to Claim 1.

Knotz teaches at col. 3, lines 52-65:

> The multilevel signal m is transmitted through the signal lead 2 to the receiver unit 3 where It is compared in the first comparator 31 with the first signal threshold V_1 above the middle logical signal level H_1, and in the second comparator 32 With the second signal threshold V_2 below the middle logical signal level H_1. As the result of comparison, the first comparator 31 supplies the first digital received signal s_{31} corresponding to the first digital transmission signal s_{11} and the second comparator 32 supplies the regenerated clock signal SC', i.e., the second digital received signal s_{32} corresponding to the second digital transmission signal s_{12} and equal to the clock signal SC.

Knotz also teaches at col. 3, lines 24-32 (emphasis added):

> For <u>amplitude filtering</u> in the receiver unit 3, one comparator 31, 32, ... 3n is provided for each of the digital transmission signals s_{11}, s_{12} ... s_{1n} respectively to compare the multilevel signal m with in each case one signal threshold V_1, V_2, ... V_n respectively between two adjacent logical signal levels of the multilevel signal m, and to supply as comparison result the digital received signal s_{31}, s_{32}, ... s_{3n} corresponding to the respective digital transmission signal s_{11}, s_{12}, ... s_{1n}..

As can be clearly seen, each of the comparators 31-3n of Knotz simply generates an output by comparing a voltage of the multilevel signal m to a reference voltage. However, the outputs of the comparators 31-3n in no way represent an "indication of frequency deviation" as required by the claim. As clearly shown in Figure 3 of Knotz, the different reference voltages of Knotz simply represent possible voltage levels within the multilevel signal m. The different reference voltages of Knotz are not used in any way to indicate a "frequency deviation" of a signal. As a result, Knotz

fails to disclose, teach, or suggest "at least two comparators," each of which is operative "to compare [a] pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation" as recited in Claim 15.

The comparators 31-3n of Knotz are used for a purpose completely unrelated to any function of APA. The comparators 31-3n of Knotz are specifically used to allow multiple digital signals to be summed and transmitted over a single lead. The comparators 31-3n of Knotz must be used in order for the multiple digital signals to be recovered from the multilevel signal m at the receiver 3. This functionality is not needed in APA in any way. The high frequency clock counter 24 of APA outputs a single value to the comparator 27. APA never teaches or suggests that the high frequency clock counter 24 needs to simultaneously output multiple values over a single lead. As a result, there is no need, teaching, or suggestion to incorporate the comparators 31-3n of Knotz into the system of APA. Knotz's Figure 3, reproduced above with relation to Claim 1, shows signal s31, the output of comparator 31, as compared to signal m, the input to comparator 31.

Examiner Luu's response in the final Office Action indicates that the Examiner misunderstands the teachings of Knotz. Knotz clearly teaches in col. 3, lines 24-32 (reproduced above) that the comparators function to provide an amplitude filtering of the multilevel signal m. As can be seen, the signals s31, s32, . . . s3n are the result of an amplitude filtering - also illustrated clearly in Knotz's Figure 3 - and have nothing to do with an "indication of frequency deviation." Knotz does not teach or suggest anything related to frequency deviation, and in fact does not mention frequency at all.

Examiner Luu also states, incorrectly and without basis, that "figure 3 of Knotz clearly indicates a frequency that a reference signal (i.e., signal m) is above a first threshold V1 (i.e. signal S31) and a frequency that a reference signal is above a second threshold V2 (i.e. signal SC'). Therefore, the outputs of the comparators indicate changes of the frequency of the input signal with respect to predetermined values V1 and V2" (page 6, second paragraph of final Office Action). Signal m is amplitude filtered, and the voltage thresholds are not at all compared with the frequency of signal m. Examiner Luu evidently confuses amplitude and frequency in Knotz's teachings and has been unable or unwilling to clarify this reasoning.

Independent Claim 15 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 16

Claim 16 requires, among other limitations, "a storage and logic module (SLM), wherein said RWG, said MCC and said comparators are operative to function periodically and the SLM is operative to store one or more indications output by the comparators, the one or more stored indications being available for readout".

This limitation is not taught or suggested by any combination of APA and Knotz in combination with the limitations of the parent claim. As Claim 16 depends from Claim 15, the arguments above with regard to Claim 15 apply here as well and are incorporated herein by reference.

Claim 16 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 17

Claim 17 requires, among other limitations, that the "SLM is further operative to process the one or more stored indications to obtain statistical information about the frequency of any of the at least one monitored clock".

This limitation is not taught or suggested by any combination of APA and Knotz, particularly in combination with the limitations of the parent claim. As Claim 17 depends from Claim 16, the arguments above with regard to Claims 15 and 16 apply here as well and are incorporated herein by reference.

In the rejection of Claims 3 and 4, Examiner Luu alleged that Knotz's element 6 functioned as the claimed storage and logic module (SLM). Examiner Luu then admits that the limitations of claim 17 are not met:

> As to claims 3 and 4, element 6 of Knotz is a simple latch wherein information is process [*sic*] based on one parameter (i.e., Data input at node D). However, it is common nowadays to have a simple miniature processor to analyze data for statistically [*sic*] purposes. This it would have been obvious to one of skill in the art to replace a simple latch with an off-the-shelf processor to process information or data as required by the claim.

Examiner Luu's argument has numerous problems. First, nothing in any art of reference teaches or suggests the desirability of making a modification to replace Knotz's latch with a processor. The only motivation suggested by Examiner Luu is "to process information or data as required by the claim," a clear indication of improper hindsight reasoning. Finally, Examiner Luu only alleges that the use of such a processor is "common nowadays". This does not even meet the requirements for a *prima facie* obviousness rejection, which requires an examination of the knowledge of one of ordinary skill in the art at the time the invention was made, not "nowadays" as the claim is being examined.

Claim 17 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 18

Claim 18 requires, among other limitations, that the "statistical information includes indication of a trend in frequency deviation".

This limitation is not taught or suggested by any combination of APA and Knotz, particularly in combination with the limitations of the parent claim. As Claim 18 depends from Claim 17, the arguments above with regard to Claims 15, 16, and 17 apply here as well and are incorporated herein by reference.

Neither Knotz nor APA teaches or suggests anything related to frequency deviation, nor anything related to statistical information at all.

Claim 18 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 19

Claim 19 requires, among other limitations, "at least one clock generator and wherein an output of any of said at least one clock generator is one of the at least one monitored clock".

This limitation is not taught or suggested by any combination of APA and Knotz in combination with the limitations of the parent claim. As Claim 19 depends from Claim 15, the arguments above with regard to Claim 15 apply here as well and are incorporated herein by reference.

Claim 19 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 20

Claim 20 requires, among other limitations, that the "at least one clock generator includes a phase locked loop (PLL)".

This limitation is not taught or suggested by any combination of APA and Knotz, particularly in combination with the limitations of the parent claim. As Claim 20 depends from Claim 19, the arguments above with regard to Claims 15 and 19 apply here as well and are incorporated herein by reference.

Claim 20 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 21

Claim 21 requires, among other limitations, that the at least one clock generator is a frequency multiplier".

This limitation is not taught or suggested by any combination of APA and Knotz, particularly in combination with the limitations of the parent claim. As Claim 21 depends from Claim 19, the arguments above with regard to Claims 15 and 19 apply here as well and are incorporated herein by reference.

Claim 21 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 22

Claim 22 requires, among other limitations, said RWG and said MCC form part of said frequency multiplier".

This limitation is not taught or suggested by any combination of APA and Knotz, particularly in combination with the limitations of the parent claim. As Claim 22 depends from Claim 21, the arguments above with regard to Claims 15, 19, and 21 apply here as well and are incorporated herein by reference.

Claim 8 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 23

Claim 23 requires, among other limitations, that "said RWG includes a reference clock counter (RCC) operative to count a given number of reference clock pulses, and wherein a beginning

of said reference window coincides with a beginning of said counting and an end of said reference window coincides with an end of said counting".

This limitation is not taught or suggested by any combination of APA and Knotz in combination with the limitations of the parent claim. As Claim 23 depends from Claim 15, the arguments above with regard to Claim 15 apply here as well and are incorporated herein by reference.

Claim 23 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 24

Claim 24 requires, among other limitations, that "a clock generator of a frequency multiplier type, whose output is a monitored clock, wherein said RCC and said MCC form part of said clock generator".

This limitation is not taught or suggested by any combination of APA and Knotz in combination with the limitations of the parent claim. As Claim 24 depends from Claim 23, the arguments above with regard to Claims 15 and 23 apply here as well and are incorporated herein by reference.

This limitation has never been addressed by Examiner Luu at all. Examiner Luu made a blanked statement, in the final rejection, that this claim (and others) are similar to Claims 11-14, but nothing like this limitation is found in Claims 11-14. There has not even been a *prima facie* rejection of this claim.

Claim 24 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Ground of Rejection 2: Claims 11-14 and 25-28 were rejected under 35 U.S.C. 103(a) as obvious over Applicant's Admitted Prior Art (APA) in view of U.S. Patent No. 6,289,055 to Knotz ("Knotz") in further view of U.S. Patent No. 6,542,013 to Volk, *et al.* ("Volk").

These claims are allowable over the art of record, as discussed below.

Claim 11

Claim 11 requires, among other limitations, that the "at least one clock is at least two clocks, the FMC further comprising a selector operative to switch any one of the at least two clocks into said MCC".

This limitation is not taught or suggested by any combination of APA, Knotz, and Volk, particularly in combination with the limitations of the parent claim. Volk also does not include the teachings discussed above as missing from the proposed APA-Knotz combination. As Claim 11 depends from Claim 1, the arguments above with regard to Claim 1 apply here as well and are incorporated herein by reference.

Volk does teach a PLL circuit 210 with a voltage controlled oscillator 212. The VCO 212 is connected to a multiplexer 208 to allow a selection of phase-shifted signals from VCO 212.

There is, however, no motivation at all to combine this with the teachings of APA and Knotz, alone or in combination. Examiner Luu's only stated "motivation" is "since Volk is capable of providing various clock signals from a single clock generator such that cost and space of the circuit can be reduced." This might be a proper motivation to look to Volk for a circuit that had multiple clocks each generating a phase-shifted output of the same clock signal, but this is not the case in APA or Knotz. In fact, Volk does not teach "at least two clocks" as claimed but simply one clock with phase-shifting circuitry. As such, even the proposed combination does not meet the plain limitations of the claim.

Claim 11 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 12

Claim 12 requires, among other limitations, that the circuit is "formed on an integrated circuit chip that forms part of a digital system and at least one of the monitored clocks is input to the chip".

This limitation is not taught or suggested by any combination of APA, Knotz, and Volk, particularly in combination with the limitations of the parent claim. Volk also does not include the teachings discussed above as missing from the proposed APA-Knotz combination. As Claim 12 depends from Claim 11, the arguments above with regard to Claims 1 and 11 apply here as well and are incorporated herein by reference.

Examiner Luu admits that this feature is not taught or suggested by the art of record, but states "they are commonly form [*sic*] on the same IC for the advatage of uniform temperature variation and to reduce variation in the fabricating process." Examiner Luu ignores the limitation that "at least one of the monitored clocks is input to the chip" and so fails to make even a *prima facie* obviousness rejection.

Claim 12 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 13

Claim 13 requires, among other limitations, that "the duration of said reference window is different for each monitored clock". This limitation is not taught or suggested by any combination of APA, Knotz, and Volk, particularly in combination with the limitations of the parent claim. Volk also does not include the teachings discussed above as missing from the proposed APA-Knotz combination. As Claim 13 depends from Claim 11, the arguments above with regard to Claim 1 and 11 apply here as well and are incorporated herein by reference.

Examiner Luu claims that this limitation is obvious because "it is obvious that the duration of the reference window being [*sic*] differeint for each monitored clock since each clock has its frequency different from the others." Examiner Luu is mistaken – Examiner Luu has argued that the

multiple "monitored clocks" is as taught by Volk, and Volk teaches a single clock with multiple phase-shifted outputs. As is readily understood by those of skill in the art, multiple phase-shifted copies of the same clock signal would have an identical frequency since the clock signals only differ in phase.

Claim 13 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 14

Claim 14 requires, among other limitations, that "for any of said comparators, the respective threshold value is different for each monitored clock".

This limitation is not taught or suggested by any combination of APA, Knotz, and Volk, particularly in combination with the limitations of the parent claim. Volk also does not include the teachings discussed above as missing from the proposed APA-Knotz combination. As Claim 14 depends from Claim 11, the arguments above with regard to Claims 1 and 11 apply here as well and are incorporated herein by reference.

Examiner Luu states that "Knotz discloses in column 3, lines 27-29 that the threshold value of V1 and V2 are different." This is true, but irrelevant. The limitation requires not that the threshold values of the multiple comparators be different from each other, but that the values be different for each monitored clock. This is not taught or suggested by any cited reference, alone or in combination. Since the only multiple clocks alleged by Examiner Luu are the phase-shifted identical clock signals of Volk, there is no point in varying the threshold values.

Claim 14 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 25

Claim 25 requires, among other limitations, that the at least one clock is at least two clocks, the FMC further comprising a selector operative to switch any one of the at least two clocks into the MCC".

This limitation is not taught or suggested by any combination of APA, Knotz, and Volk, particularly in combination with the limitations of the parent claim. Volk also does not include the teachings discussed above as missing from the proposed APA-Knotz combination. As Claim 25 depends from Claim 15, the arguments above with regard to Claim 15 apply here as well and are incorporated herein by reference.

Volk does teach a PLL circuit 210 with a voltage controlled oscillator 212. The VCO 212 is connected to a multiplexer 208 to allow a selection of phase-shifted signals from VCO 212.

There is, however, no motivation at all to combine this with the teachings of APA and Knotz, alone or in combination. Examiner Luu's only stated "motivation" is "since Volk is capable of providing various clock signals from a single clock generator such that cost and space of the circuit can be reduced." This might be a proper motivation to look to Volk for a circuit that had multiple clocks each generating a phase-shifted output of the same clock signal, but this is not the case in APA or Knotz. In fact, Volk does not teach "at least two clocks" as claimed but simply one clock with phase-shifting circuitry. As such, even the proposed combination does not meet the plain limitations of the claim.

Claim 25 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 26

Claim 26 requires, among other limitations, "the chip forming part of a digital system and at least one of the monitored clocks being generated, within the system, outside the chip".

This limitation is not taught or suggested by any combination of APA, Knotz, and Volk, particularly in combination with the limitations of the parent claim. Volk also does not include the

teachings discussed above as missing from the proposed APA-Knotz combination. As Claim 26 depends from Claim 25, the arguments above with regard to Claims 15 and 25 apply here as well and are incorporated herein by reference.

Examiner Luu admits that this feature is not taught or suggested by the art of record, but states "they are commonly form [*sic*] on the same IC for the advatage of uniform temperature variation and to reduce variation in the fabricating process." Examiner Luu ignores the limitation that "at least one of the monitored clocks is input to the chip" and so fails to make even a *prima facie* obviousness rejection.

Claim 26 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 27

Claim 27 requires, among other limitations, that "the duration of said reference window is different for each monitored clock". This limitation is not taught or suggested by any combination of APA, Knotz, and Volk, particularly in combination with the limitations of the parent claim. Volk also does not include the teachings discussed above as missing from the proposed APA-Knotz combination. As Claim 27 depends from Claim 25, the arguments above with regard to Claim 15 and 25 apply here as well and are incorporated herein by reference.

Examiner Luu claims that this limitation is obvious because "it is obvious that the duration of the reference window being [*sic*] differeint for each monitored clock since each clock has its frequency different from the others." Examiner Luu is mistaken – Examiner Luu has argued that the multiple "monitored clocks" is as taught by Volk, and Volk teaches a single clock with multiple phase-shifted outputs. As is readily understood by those of skill in the art, multiple phase-shifted copies of the same clock signal would have an identical frequency since the clock signals only differ in phase.

Claim 27 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Claim 28

Claim 28 requires, among other limitations, that "for any of said comparators, the respective threshold value is different for each monitored clock".

This limitation is not taught or suggested by any combination of APA, Knotz, and Volk, particularly in combination with the limitations of the parent claim. Volk also does not include the teachings discussed above as missing from the proposed APA-Knotz combination. As Claim 28 depends from Claim 25, the arguments above with regard to Claims 15 and 25 apply here as well and are incorporated herein by reference.

Examiner Luu states that "Knotz discloses in column 3, lines 27-29 that the threshold value of V1 and V2 are different." This is true, but irrelevant. The limitation requires not that the threshold values of the multiple comparators be different from each other, but that the values be different for each monitored clock. This is not taught or suggested by any cited reference, alone or in combination. Since the only multiple clocks alleged by Examiner Luu are the phase-shifted identical clock signals of Volk, there is no point in varying the threshold values.

Claim 28 is therefore allowable over all art of record, alone or in combination. Applicant respectfully requests that Examiner Luu's rejections be reversed, and this case be returned to the Examiner for allowance.

Motivation to Combine or Modify[2]

As described above with regard to particular claims, even if the combination of references did teach all limitations of the claims – and they do not – the obviousness rejections must fail as lacking motivation or based on improper motivation.

For example, the motivation stated for Examiner Luu's proposed APA-Knotz combination is "for the benefit of determining a specific range or bandwidth of the pulse signal". This motivation is not supported in the art. The claim limitations require multiple comparators that output an indication of frequency deviation. To meet this limitation, Examiner Luu proposes combining a multiple-comparator amplitude filter from Knotz with prior art Figure 2. While this would determine a specific amplitude range of the clock signal of Figure 2, there is no teaching or suggestion in the art that this is desirable. This combination would not, however, meet the claim limitations. The generic motivation stated by the Examiner would not motivate one of skill in the art to reproduce the claimed inventions from any combination of cited references.

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[2]Where an obviousness rejection is based on a combination of references, the Examiner must show that one of ordinary skill would have been motivated to combine those references. *See In re Nilssen*, 7 USPQ2d 1500 (Fed.Cir. 1988); *Panduit Corp. v. Dennison Mfg. Co.*, 1 USPQ2d 1593, 1597 (Fed.Cir. 1987); *ACS Hospital Systems v. Montefiore Hospital*, 220 USPQ 929 (Fed.Cir. 1984).

"When prior art references require selective combination ... to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself.... Something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination." *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 5 USPQ2d 1434, 1438 (Fed.Cir. 1988), *quoting Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed.Cir. 1985), *and Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick*, 221 USPQ 481 (Fed.Cir. 1984).

"While *[a reference]* may be capable of being modified to run the way *[the applicant's]* apparatus is claimed, there must be a suggestion or motivation in the reference to do so. See In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) ("The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification."). *In re Mills,* 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed.Cir. 1990).

The "motivation" alleged by the Examiner is "since it would provide different readings in at the same moment" (page 3, second paragraph of final Office Action). The Examiner acknowledges that "[t]he combination of prior arts is based on general knowledge, and not based on Applicant's disclosure" (page 6, first paragraph). Clearly, there is also no such motivation taught in Knotz, and the law is clear that the motivation to combine or modify must be specific to the actual teachings sought to be combined. "When the references are in the same field as that of the applicant's invention, knowledge thereof is presumed. However, the test of whether it would have been obvious to select specific teachings and combine them as did the applicant must still be met by identification of some suggestion, teaching, or motivation in the prior art, arising from what the prior art would have taught a person of ordinary skill in the field of the invention." (*In re Dance*, 160 F.3d 1339, 1343 (Fed. Cir. 1998), emphasis added). As Examiner Luu's "general knowledge" statement of motivation is does not teach making any specific modification at all, this rejection is legally deficient.

The Examiner seeks to combine the references by combining Knotz's dual-comparator amplitude filter and use it in the circuit as disclosed in APA. Nothing in the cited art, or in the knowledge of those of skill in the art, suggests that adding an amplitude filter to the APA circuit would have any utility whatsoever. Nothing of "general knowledge", as alleged by the Examiner, would suggest looking to Knotz's amplitude filter for any purpose in the APA circuit.

Although Applicant has challenged Examiner Luu's factual assertion as not properly officially noticed or not properly based upon common knowledge, Examiner Luu has refused to support the finding with adequate evidence as required by MPEP 2144.03.

Further, the motivation to combine APA-Knotz for "multiple clock signals" is addressed above with regard to Claims 11 and 25.

Grouping of Claims

The claims on appeal do not stand or fall together, as may be seen from the arguments set forth below. Each claim has been argued separately under a separate subheading, and each claim should be considered separately. While the applicant recognizes that a formal statement regarding the grouping of claims is no longer required, each claim should be considered separately; or at the very least each claim which is argued separately in the preceding sections of this brief should be considered separately. Argument: The fact that the claims use different formulations (as detailed above) and/or have been argued separately, shows that, if their patentability is not considered separately, any adverse decision would show that the limitations of some claims had been unfairly ignored.

REQUESTED RELIEF

The Board is respectfully requested to reverse the outstanding rejections and return this application to the Examiner for allowance.

Respectfully submitted,

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Date: Dec 6, 2006

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DOCKET NO. P05411 **PATENT**
CLIENT NO. NATI15-05411
Customer No. 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Moshe Alon
Serial No.:	10/797,478
Filed:	March 10, 2004
For:	CLOCK FREQUENCY MONITOR
Group No.:	2816
Examiner:	An T. Luu

APPENDIX A -

Claims Appendix

1. (Previously Presented) A frequency monitor circuit (FMC) configured to receive at least one monitored clock whose frequency is to be monitored, said FMC comprising:

a reference window generator (RWG) operative to output a reference window signal defining a reference window, the reference window having a given duration;

a monitored clock counter (MCC) operative to count all pulses in any one of the at least one monitored clock that occur within the duration of said reference window and to output a corresponding pulse count; and

at least two comparators, each comparator operative to compare said pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation.

2. (Previously Presented) The frequency monitor circuit of claim 1, further comprising a storage and logic module (SLM), wherein said RWG, said MCC and said comparators are operative to function repeatedly and the SLM is operative to store one or more indications output by the comparators, the one or more stored indications being available for readout.

3. (Previously Presented) The frequency monitor circuit of claim 2, wherein said SLM is further operative to process the stored indications so as to obtain statistical information about the frequency of any of the at least one monitored clock.

4. (Original) The frequency monitor circuit of claim 3, wherein said statistical information includes indication of a trend in frequency deviation.

5. (Previously Presented) The frequency monitor circuit of claim 1, formed on an integrated circuit chip that includes at least one clock generator, an output of any of said at least one clock generator being one of the at least one monitored clock.

6. (Previously Presented) The frequency monitor circuit of claim 5, wherein said at least one clock generator comprises a phased locked loop (PLL).

7. (Previously Presented) The frequency monitor circuit of claim 5, wherein said at least one clock generator is a frequency multiplier.

8. (Original) The frequency monitor circuit of claim 7, wherein said RWG and said MCC form part of said frequency multiplier.

9. (Previously Presented) The frequency monitor circuit of claim 1, wherein said RWG includes a reference clock counter (RCC) operative to count a given number of reference clock pulses in a reference clock, and wherein a beginning of said reference window coincides with a beginning of said counting and an end of said reference window coincides with an end of said counting.

10. (Previously Presented) The frequency monitor circuit of claim 9, wherein an integrated circuit chip includes a clock generator of a frequency multiplier type, whose output is a monitored clock, wherein said RCC and said MCC form part of said clock generator.

11. (Previously Presented) The frequency monitor circuit of claim 1, wherein said at least one clock is at least two clocks, the FMC further comprising a selector operative to switch any one of the at least two clocks into said MCC.

12. (Original) The frequency monitor circuit of claim 11, formed on an integrated circuit chip that forms part of a digital system and at least one of the monitored clocks is input to the chip.

13. (Original) The frequency monitor circuit of claim 11, wherein the duration of said reference window is different for each monitored clock.

14. (Original) The frequency monitor circuit of claim 11, wherein, for any of said comparators, the respective threshold value is different for each monitored clock.

15. (Previously Presented) An integrated circuit chip, on which there is provided at least one monitored clock whose frequency is to be monitored, the chip comprising a frequency monitor circuit (FMC) that includes:

a reference window generator (RWG) operative to output a reference window signal defining a reference window, the reference window having a given duration;

a monitored clock counter (MCC) operative to count all pulses in any one of the at least one monitored clock that occur within the duration of said reference window and to output a corresponding pulse count; and

at least two comparators, each comparator operative to compare said pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation.

16. (Previously Presented) The integrated circuit chip of claim 15, wherein said FMC further includes a storage and logic module (SLM), wherein said RWG, said MCC and said comparators are operative to function periodically and the SLM is operative to store one or more indications output by the comparators, the one or more stored indications being available for readout.

17. (Previously Presented) The integrated circuit chip of claim 16, wherein said SLM is further operative to process the one or more stored indications to obtain statistical information about the frequency of any of the at least one monitored clock.

18. (Original) The integrated circuit chip of claim 17, wherein said statistical information includes indication of a trend in frequency deviation.

19. (Previously Presented) The integrated circuit chip of claim 15, further including at least one clock generator and wherein an output of any of said at least one clock generator is one of the at least one monitored clock.

20. (Previously Presented) The integrated circuit chip of claim 19, wherein said at least one clock generator includes a phase locked loop (PLL).

21. (Previously Presented) The integrated circuit chip of claim 19, wherein said at least one clock generator is a frequency multiplier.

22. (Original) The integrated circuit chip of claim 21, wherein said RWG and said MCC form part of said frequency multiplier.

23. (Previously Presented) The integrated circuit chip of claim 15, wherein there is further provided on the chip a reference clock, wherein said RWG includes a reference clock counter (RCC) operative to count a given number of reference clock pulses, and wherein a beginning of said reference window coincides with a beginning of said counting and an end of said reference window coincides with an end of said counting.

24. (Previously Presented) The integrated circuit chip of claim 23, further including a clock generator of a frequency multiplier type, whose output is a monitored clock, wherein said RCC and said MCC form part of said clock generator.

25. (Previously Presented) The integrated circuit chip of claim 15, wherein said at least one clock is at least two clocks, the FMC further comprising a selector operative to switch any one of the at least two clocks into the MCC.

26. (Original) The integrated circuit chip of claim 25, the chip forming part of a digital system and at least one of the monitored clocks being generated, within the system, outside the chip.

27. (Previously Presented) The integrated circuit chip of claim 25, wherein the duration of said reference window is different for each monitored clock.

28. (Previously Presented) The integrated circuit chip of claim 25, wherein, for any of said comparators, the respective threshold value is different for each monitored clock.

DOCKET NO. P05411 **PATENT**
CLIENT NO. NATI15-05411
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Moshe Alon
Serial No.:	10/797,478
Filed:	March 10, 2004
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Examiner:	An T. Luu

APPENDIX B
Evidence Appendix

None.

DOCKET NO. P05411 **PATENT**
CLIENT NO. NATI15-05411
Customer No. 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Moshe Alon
Serial No.:	10/797,478
Filed:	March 10, 2004
For:	CLOCK FREQUENCY MONITOR
Group No.:	2816
Examiner:	An T. Luu

APPENDIX C

One set of Formal Drawings

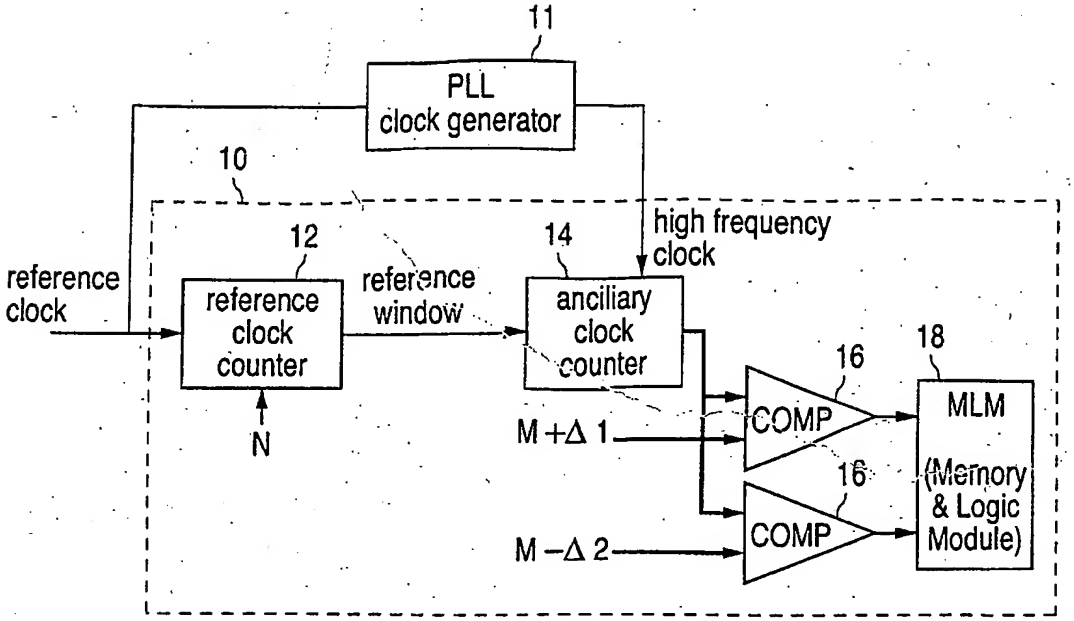
11
PLL
clock generator
10
high frequency
clock
12
14
reference
clock
reference
clock
counter
reference
window
anciliary
clock
counter
16
18
COMP
MLM
(Memory
& Logic
Module)
N
M +Δ 1
16
COMP
M −Δ 2

FIG. 1A

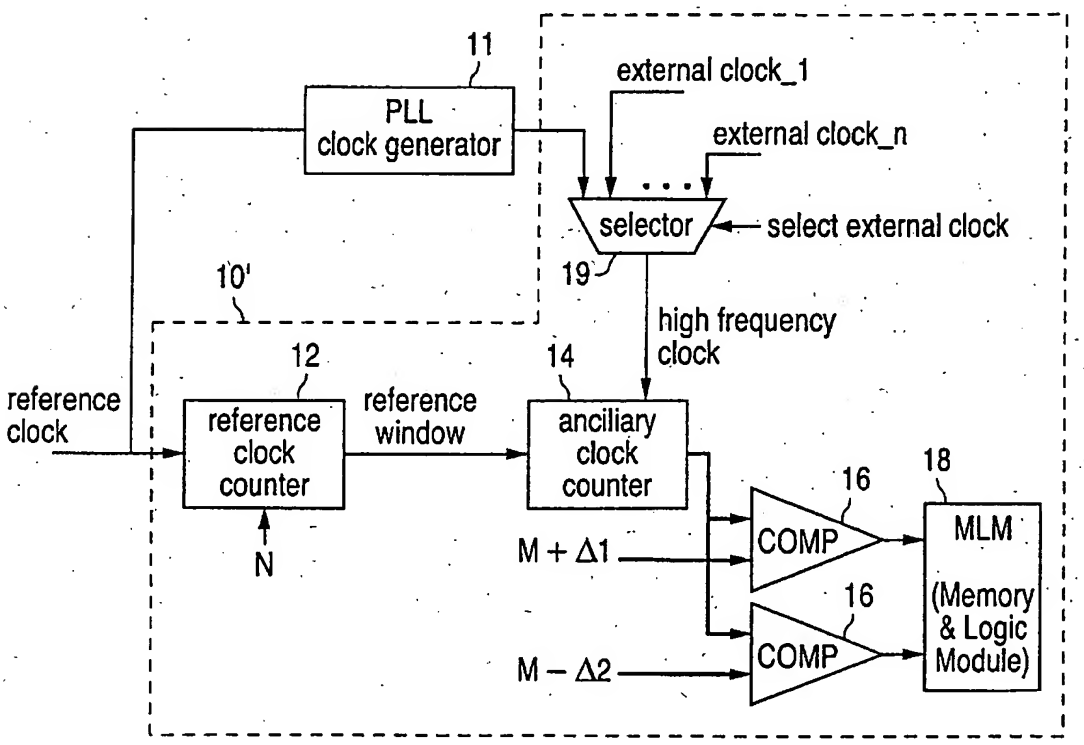
11
external clock_1
PLL
clock generator
external clock_n
selector
select external clock
19
10'
high frequency
clock
12
14
reference
clock
reference
clock
counter
reference
window
anciliary
clock
counter
16
18
COMP
MLM
(Memory
& Logic
Module)
N
M + Δ1
16
COMP
M − Δ2

FIG. 1B

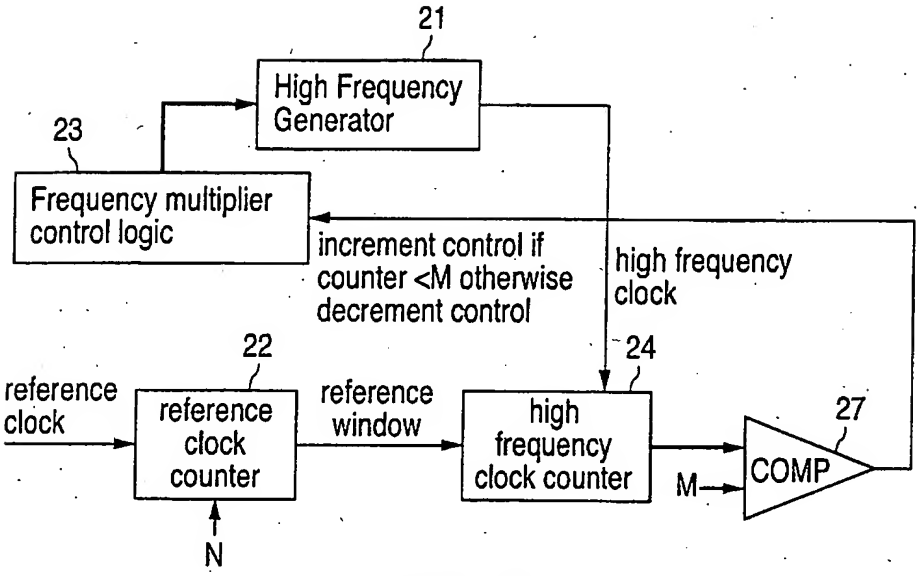

FIG. 2
(PRIOR ART)

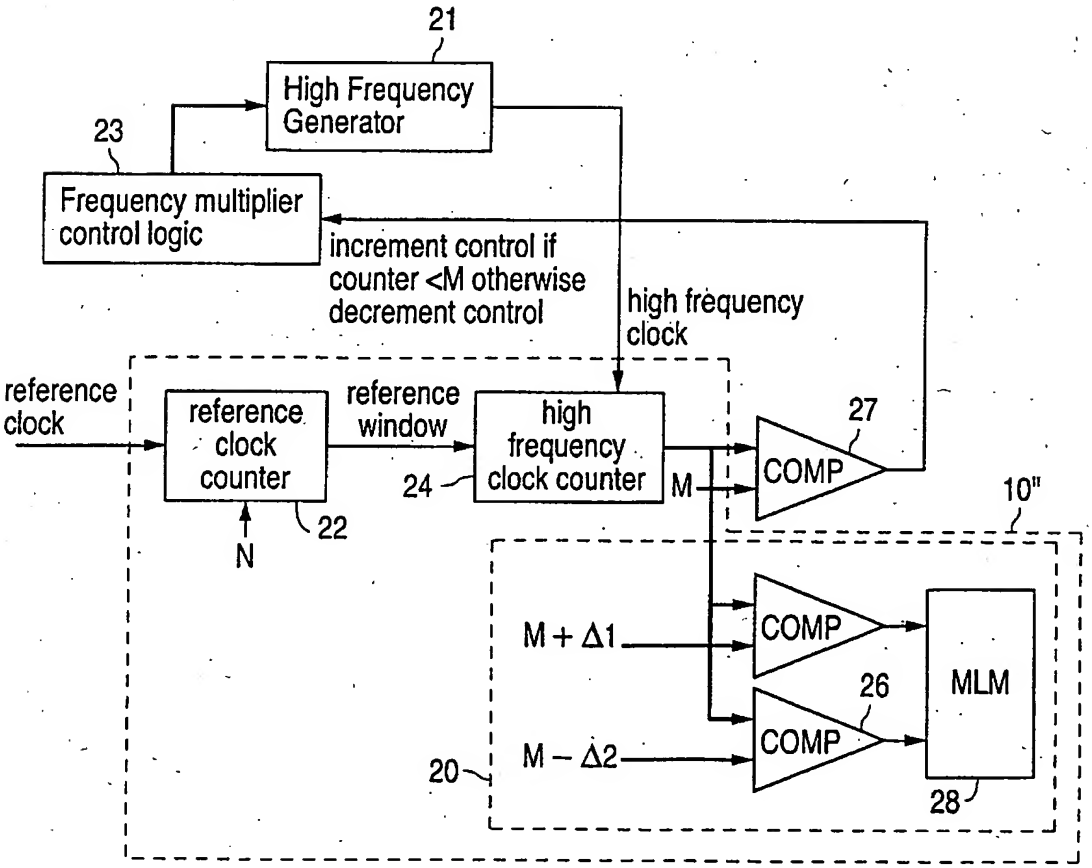

FIG. 3

DOCKET NO. P05411 **PATENT**
CLIENT NO. NATI15-05411
Customer No. 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APPENDIX D
Related Proceedings Appendix

Not Applicable – To the best knowledge and belief of the undersigned attorney, there are none.